Amendments to the Drawings:

The attached drawing sheets include changes to Figs. 5 and 10. In Fig. 5, the signal connections of CMN and CMNbar to transistors MP1 & 2 and MN1 & 2 are amended. In Fig. 10, reference numeral designations are added to specifically identify the gate and body connections of the transistors.

REMARKS/ARGUMENTS

In the Office Action mailed January 27, 2009, claims 1-4 and 7-14 were rejected. Additionally, the drawings were objected to. In response, Applicants hereby request reconsideration of the application in view of the below-provided remarks. No claims are amended, added, or canceled.

Objections to the Drawings

The Office Action states that Figure 5 is objected to because the signal connections of CMN and CMNbar to transistors MP1 & 2 and MN1 & 2 are unclear. Applicants submit Figure 5 is amended to clarify the signal connections of CMN and CMNbar to transistors MP1 & 2 and MN1 & 2. Accordingly, Applicants respectfully request that the objection to Figure 5 be withdrawn.

The Office Action states that Figure 10 is objected to because the gate and body connections of the transistors of Figure 10 are not clear and should be represented more clearly. Applicants submit Figure 10 is amended to clarify the gate and body connections of the transistors of Figure 10, and corresponding language is added to the specification to describe what is already illustrated in Figure 10. Accordingly, Applicants respectfully request that the objection to Figure 10 be withdrawn.

Claim Rejections under 35 U.S.C. 102 and 103

Claims 1-4, 7, 8, and 12-14 were rejected under 35 U.S.C. 102(a) as being anticipated by Chung et al. (U.S. Pat. No. 7,035,148, hereinafter Chung). Additionally, claims 9 and 10 were rejected under 35 U.S.C. 103(a) as being unpatentable over Chung in view of Ajit (U.S. Pat. Pub. No. 2002/0113628, hereinafter Ajit). Additionally, claim 11 was rejected under 35 U.S.C. 103(a) as being unpatentable over Chung in view of Schultz (U.S. Pat. No. 6,445,245, hereinafter Schultz). However, Applicants respectfully submit that these claims are patentable over Chung, Ajit, and Schultz for the reasons provided below.

Independent Claim 1

Claim 1 recites "load determination means for determining a load" (emphasis added). Additionally, claim 1 recites "adjusting means for switching off a buffer connected to the configurable circuit according to the determination of the applied load, wherein switching off the buffer adjusts a drive capacity of said at least one circuit component to a value less than a maximum drive capacity while still meeting a delay specification" (emphasis added).

In contrast, Chung does not disclose all of the limitations of the claim. In particular, Chung does not disclose determining a load, as recited in the claim. Also, Chung does not disclose switching off a buffer, as recited in the claim. More specifically, Chung does not disclose switching off a buffer to adjust a drive capacity, as recited in the claim. Each of these shortcomings in the disclosure of Chung is separately addressed below.

A. Chung does not disclose determining a load.

Chung does not disclose determining a load. Chung generally describes adjusting a slew rate. Chung, abstract. More specifically, Chung teaches that a mode register set (MRS) 15 stores column address select (CAS) latency information. Chung col. 2, line 8, to col. 3, line 30. A control circuit 17 reads the CAS latency information stored in the MRS 15 and generates control signals. Id. Driving capabilities of pull-up driver 11 and pull-down driver 13 are then varied in response to the control signals. Id. The Office Action purports that the MRS 15 of Chung determines a load. Office Action, page 3.

However, the MRS 15 lacks any type of determination function according to the disclosure of Chung. Chung discloses that the MRS 15 stores CAS latency information. In fact, the only disclosed function of the MRS 15 is to store information. Storing information is different from determining information because the act of storing information involves storing information previously known or already determined.

Moreover, even if Chung were to disclose determining information, nevertheless, Chung appears silent with regard to determining a load. Hence, Chung does not disclose a load determination means for determining a load, as recited in the claim.

For the reasons presented above, Chung does not disclose all of the limitations of the claim because Chung does not disclose determining a load, as recited in the claim. Accordingly, Applicants respectfully assert claim 1 is patentable over Chung because Chung does not disclose all of the limitations of the claim.

B. Chung does not disclose switching off a buffer.

Additionally, Chung does not disclose switching off a buffer. The Office Action purports that the control circuit 17 of Chung switches off a buffer. Office Action, page 3. As explained above, the control circuit 17 generates control signals. Chung col. 2, line 8, to col. 3, line 30. Pull-up and pull-down transistors are then selectively enabled in response to the control signals. Id. However, the pull-up and pull-down transistors of Chung do not appear to relate to a buffer. In fact, the disclosure of Chung does not mention a buffer.

The Office Action appears to assert that the mere use of a p-channel and n-channel transistor pair in series constitutes a buffer. However, the Office Action provides no basis in the form of a reference, or other evidence, to support this assertion. Further, there appears to be no reference to a p-channel and n-channel transistor pair in series constituting a buffer in and of themselves. Although transistor pairs may be used with additional components to constitute a certain type of buffer, the mere use of a pair of transistors alone does not typically constitute a buffer.

Therefore, with regard to the control circuit 17 enabling p-channel and n-channel transistors, Chung does not disclose switching off a buffer. However, even if the transistor pairs of Chung were to describe a buffer, nevertheless, Chung fails to disclose switching off a buffer according to a determination of an applied load. Instead, Chung discloses enabling transistor pairs according to the CAS latency information stored in the MRS 15. As explained above in Section A, CAS latency information does not relate to a load or the determination of a load. Hence, Chung does not disclose adjusting means for switching off a buffer connected to the configurable circuit according to the determination of the applied load, as recited in the claim.

For the reasons presented above, Chung does not disclose all of the limitations of the claim because Chung does not disclose switching off a buffer according to the

determination of the applied load, as recited in the claim. Accordingly, Applicants respectfully assert claim 1 is patentable over Chung because Chung does not disclose all of the limitations of the claim.

C. Chung does not disclose switching off a buffer to adjust a drive capacity.

Moreover, Chung does not disclose adjusting a drive capacity. Instead, as explained above in Section A, Chung generally describes adjusting a slew rate. Chung, abstract. More specifically, as the pull-up and pull-down transistors are selectively enabled in response to the control signals, the slew rate of a signal output from an output terminal is adjusted. Chung col. 2, line 8, to col. 3, line 30. If the CAS information stored in the MRS 15 is large (high latency), then the number of transistors enabled is increased. Id. As a result, the slew rate is decreased. Id. On the other hand, if the CAS information stored in the MRS 15 is small (low latency), then the number of enabled transistors is decreased. Id. As a result, the slew rate is increased. Id.

Chung does not describe adjusting a capacity to drive a load but rather a capacity to synchronize input and output frequencies. A slew rate does not relate to the capacity to drive a load, but rather, describes the maximum rate of change of a signal at any point in a circuit. The slew rate identifies the maximum input frequency applicable to an active component so as not to distort the output of the active component. Driving a load generally relates to electrical power, and the equation for electrical power relates to voltage and amperage over time. Frequency is not an element in the equation of electrical power. If slew rate relates to frequency and the capacity to synchronize a signal then slew rate does not relate to a capacity to drive a load. Hence, Chung does not disclose switching off the buffer adjusts a drive capacity of said at least one circuit component to a value less than a maximum drive capacity, as recited in the claim.

For the reasons presented above, Chung does not disclose all of the limitations of the claim because Chung does not disclose switching off a buffer to adjust a drive capacity, as recited in the claim. Accordingly, Applicants respectfully assert claim 1 is patentable over Chung because Chung does not disclose all of the limitations of the claim.

Independent Claim 12

Applicants respectfully assert independent claim 12 is patentable over Chung at least for similar reasons to those stated above in regard to the rejection of independent claim 1. In particular, claim 12 recites "determining a load applied to at least one circuit component having different fan-in or fan-out depending on a configuration of said configurable circuit arrangement" (emphasis added). Additionally, claim 12 recites "switching off a buffer connected to the configurable circuit according to the determination of the applied load" (emphasis added).

Here, although the language of claim 12 differs from the language of claim 1, and the scope of claim 12 should be interpreted independently of claim 1, Applicants respectfully assert that the remarks provided above in regard to the rejection of claim 1 also apply to the rejection of claim 12. Accordingly, Applicants respectfully assert claim 12 is patentable over Chung because Chung does not disclose determining a load applied to at least one circuit, as recited in the claim. Additionally, Chung does not disclose switching off a buffer connected to the configurable circuit according to the determination of the applied load, as recited in the claim.

Dependent Claims

Claims 2-4, 7-11, 13, and 14 depend from and incorporate all of the limitations of the corresponding independent claims 1 and 12. Applicants respectfully assert claims 2-4, 7-11, 13, and 14 are allowable based on allowable base claims. Additionally, each of claims 2-4, 7-11, 13, and 14 may be allowable for further reasons, as described below.

In regard to claims 8 and 14, Applicants respectfully submit that claims 8 and 14 are not anticipated by Chung because Chung does not disclose all of the limitations of the claims. Claims 8 and 14 depend from claims 7 and 13 respectively and, hence, include the same limitations through dependency. Additionally, claim 8 recites means for "deriving said control signal from a most significant bit signal of a selection signal obtained from said determination means" (emphasis added). Claim 14 recites similar limitations. In contrast, Chung merely discloses the control circuit 17 generates control signals in response to the CAS latency information stored in the MRS 15. Chung, col. 2, lines 8-14. More specifically, Table 1 of Chung shows an example of CAS latency

information stored in the MRS 15. Chung, col. 2, lines 38-39. Table 2 shows logic states of the control signals. Chung, col. 2, lines 39-42. Chung expressly discloses that the control signals displayed in Table 2 are derived from the CAS latency information displayed in Table 1. Chung, col. 2, lines 18-23. Chung does not appear to disclose that the control signals are derived from a most significant bit signal. In fact, Chung does not mention the words "bit signal" or "bit" in the disclosure. Hence, the control signals of Chung are not derived from a most significant bit signal.

Moreover, even if the Office Action were to rely on Table 2 of Chung as potentially describing derivation of a control signal from a most significant bit signal, such reliance would be misplaced. In particular, even if the a0 control signal of Table 2 of Chung were interpreted as being stored in a most significant bit position, such a basis would be incorrect to establish a disclosure of deriving a control signal from a most significant bit signal. Such a basis would confuse a control signal with a most significant bit on the one hand with a control signal derived from a most significant bit signal on the other. Nevertheless, Chung appears silent with regard to any bit being in the most significant bit position. Hence, there is no basis to say whether any control signal in Table 2 or any data stored in the MRS 15 is in the most significant bit position. Accordingly, Applicants respectfully assert that claims 8 and 14 are not anticipated by Chung because Chung does not disclose deriving a control signal from a most significant bit signal of a selection signal, as recited in claims 8 and 14.

CONCLUSION

Applicants respectfully request reconsideration of the claims in view of the remarks made herein. A notice of allowance is earnestly solicited.

At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account **50-4019** pursuant to 37 C.F.R. 1.25. Additionally, please charge any fees to Deposit Account **50-4019** under 37 C.F.R. 1.16, 1.17, 1.19, 1.20 and 1.21.

Respectfully submitted,

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